



Department of Electronics & Communication Engineering

GOVERNMENT POLYTECHNIC FOR GIRLS, SURAT

SEP -2021: Vol.-02

EC TRENDS

E-Newsletter



Vision:

Be an excellent department for girls to empower them in the field of Electronics and Communication engineering to excel in industry and serve society.

Mission:

- To prepare professionally competent students and staff through academic excellence.
- To create a conducive environment in the department for exchange of ideas and knowledge.
- To provide opportunities in the department for skill development and innovation.
- To provide resources and infrastructure for best learning experience in the department.

Message from Head of Department



Dr. S. N. Sampat

Head of the Department Electronics and
communication Engineering. ,

(I/C principal, GPG . Surat.

A digital platform will provide a more environmentally sustainable and cost-efficient way for our department to communicate with you, our valued supporters.

Over the past few months, our faculty and staff have worked tirelessly to provide an excellent educational experience for our students. While the coronavirus pandemic has had many disruptive effects, we have continued our academic offerings for students via distance learning and maintained our interactions with alumni and supporters in all possible forms, including this newsletter.

I am particularly proud of the dedication of our faculty in digitally delivering their courses, as well as the perseverance and commitment of our students in an online learning environment. No matter how long this crisis may persist, I am confident in the resilience of our program because of our dedicated faculty, our hard-working students, and our supportive alumni and friends like you.

I am hopeful we continue to follow all COVID-related safety procedures to remain healthy and safely.

Kind Regards,

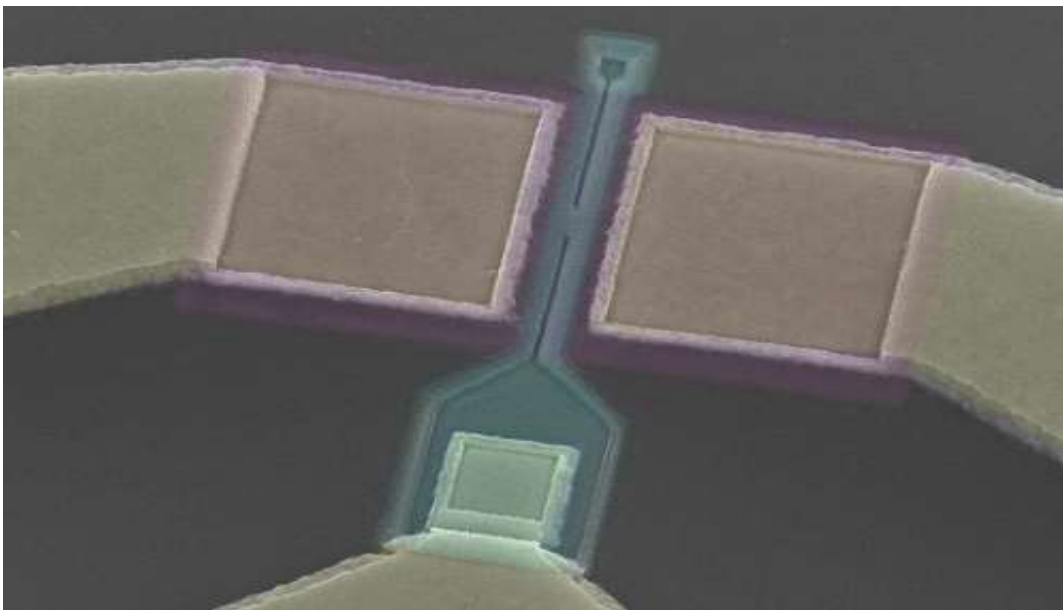
Principal of GPG, Surat.

. EFY have published a paper in ELECTRONICSFORU on JUNE 09, 2021. Here we have taken this document so that all can be aware of Trends in Electronics or Technology Field.

TRENDS IN ELECTRONICS OR TECHNOLOGY FIELD

“Hybrid III–V Tunnel FET Technology Integrated On Silicon”

Silicon-based hybrid device that combines III-V tunnel FETs and conventional MOSFETs, paving the path for future energy-efficient electronics



Scanning Electron Microscopy (SEM) showing a TFET after n^+ -InGaAs (g) and after p^+ -GaAsSb (Image credit: www.nature.com)

Innovations at the transistor level over the past few years have been at the forefront of driving the electronics industry to new heights. There has always been a need to develop fast processing electronics components that are compact at the same time.

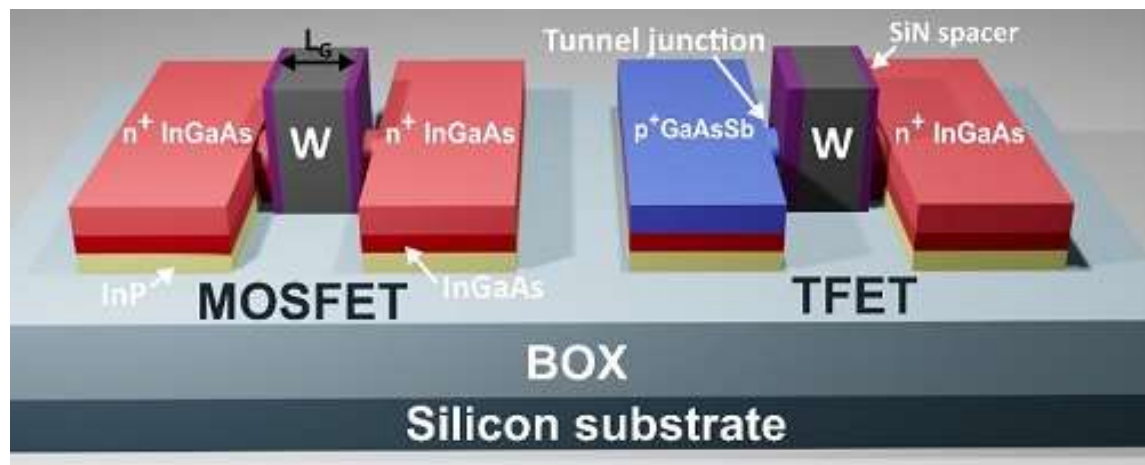
Metal-oxide-semiconductor field-effect transistors (MOSFETs) are the most conventional and widely used type of transistors. However, their high power inefficiency proves to be a limitation, which is due to their inability to reduce the voltage supply while simultaneously limiting the off-state leakage current.

The device known as a tunnel field-effect transistor (TFET) can overcome this limitation by taking advantage of quantum mechanical tunnelling instead of thermionic emission. TFETs, particularly those with a III-V heterostructure, require less than 60

mV of gate voltage swing to induce a variation of one order of magnitude in the drain current at ambient temperatures. Despite their lower power consumption, TFETs aren't yet fast and energy-efficient like MOSFETs at higher drive voltages.

Relating to this, researchers at IBM Research Europe and École Polytechnique Fédérale de Lausanne (EPFL) have recently developed a silicon-based hybrid device that combines III-V tunnel FETs and conventional MOSFETs.

“We demonstrated the first hybrid technology platform combining III-V tunnel FETs and MOSFETs with a scalable process and suitable for large-scale semiconductor manufacturing,” said Clarissa Convertino, researcher at École Polytechnique Fédérale de Lausanne. “Such low-power technology platform paves the way to future energy-efficient electronics, with the ultimate goal of reducing the carbon footprint of the ICT industry,” she said.



Three-dimensional schematic of the III–V MOSFET and TFET fabricated on silicon. The gate is made of tungsten (W). LG is the gated channel length. (Image credit: www.nature.com)

The new platform developed by Convertino and her colleagues exploits the synergies between tunnel FETs and MOSFETs, as it allows users to implement hybrid logic blocks tailored to the unique specifics of each type of device. In initial evaluations, the scaled III-V hybrid TFET-MOSFET device achieved a minimum subthreshold slope of 42 mV dec⁻¹ for TFET devices and 62 mV dec⁻¹ for MOSFET devices.

“Tunnel FETs provide lower leakage and good performance at low voltages levels, while MOSFETs are faster (at the same dimension and bias) and provide greater current drive,” Convertino explained. “The developed fabrication flow is identical for both devices except for a single masking and epitaxy step, opening up for manufacturing of truly hybrid logic blocks. Moreover, our tunnel FETs show record performance at the smallest gate length reported to our best knowledge,” she added.

The remarkable performance achieved by the device is due to the introduction of a self-aligned source-replacement step. In their platform, the position of the GaAsSb source is determined by digital etching, a process that allows the removal of material in the nanometer range.

Convertino and her colleagues demonstrated the integration of an in-plane heterojunction tunnel FET in an advanced hybrid platform using replacement metal-gate and spacer technologies. In the future, this technology could enable the development of faster and more efficient electronic devices that combine the advantages associated with TFET and MOSFET transistors.

More details about the technology have been presented in a paper published in Nature Electronics.

References:

- ✓ <https://www.electronicsforu.com/news/whats-new/hybrid-iii-v-tunnel-fet-technology-integrated-silicon>

EVENTS OF THE TERM

A wide and diversified range of extracurricular activities exists on GGP, SURAT campuses. Students become involved in extracurricular activities not only for entertainment, social, and enjoyment purposes, but most important, to gain and improve skills and offer many social opportunities while also promoting service.

Various online and offline Events are Held at institute which can be very helpful in OVER this covid -19 pandemic situation.

OFFLINE : G.P.G. SURAT, CAMPUS.

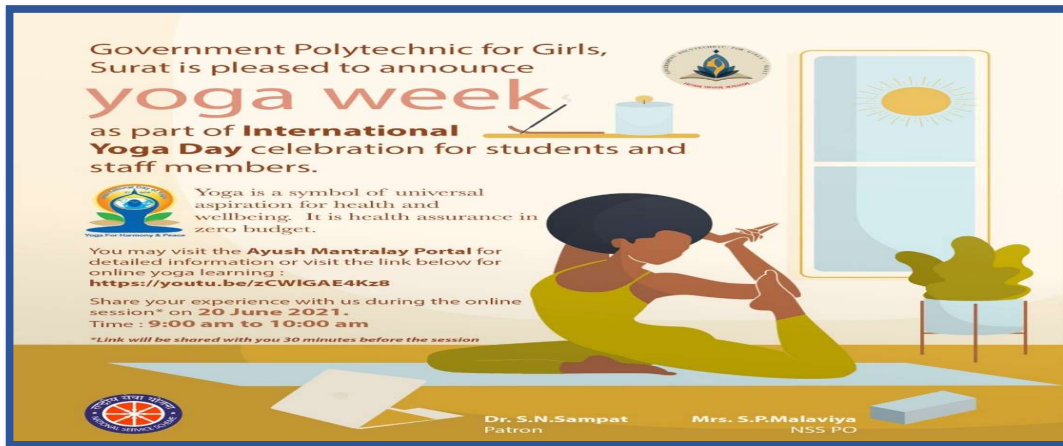
Online Mode -Microsoft Team

Date: 05/06/2021 Event Name: Tree plantation activity @ GGP, SURAT campus.

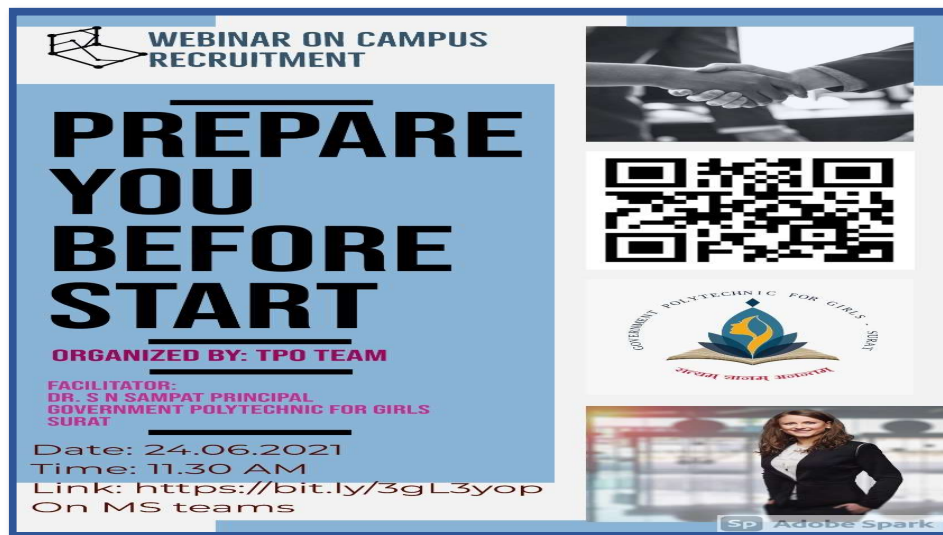


**Date: 17/06/2021 Event Name: Webinar on Post Covid Respiratory Rehabilitation
Mode of Conduct: Online**



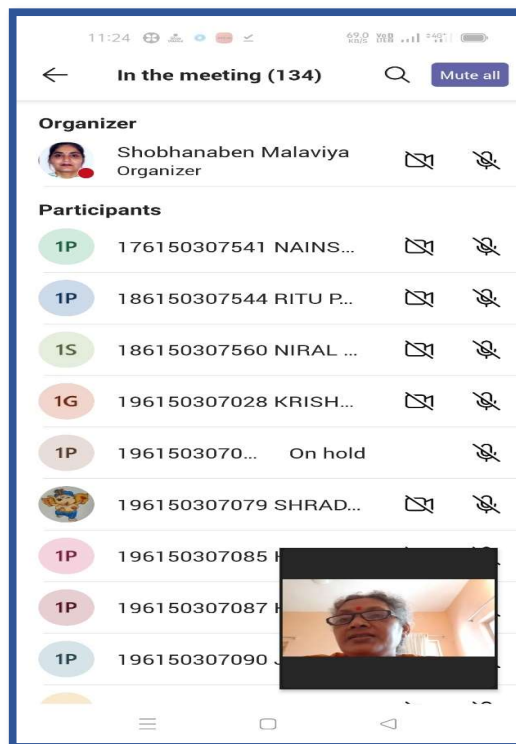
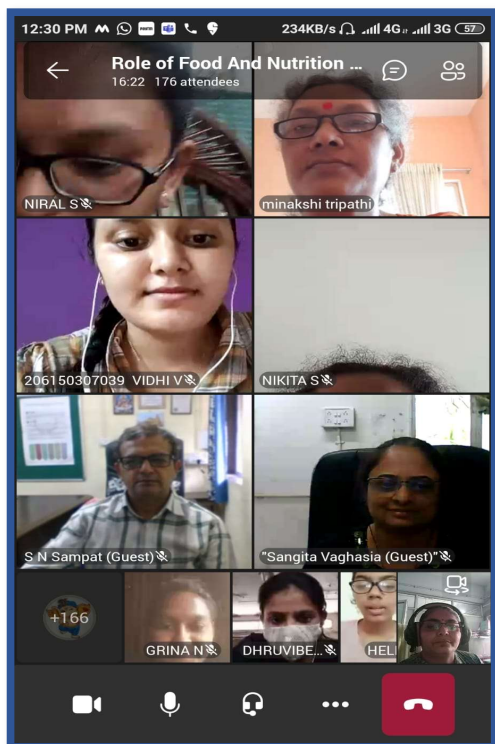


Date: 20/06/2021 Event Name: “INTERNATIONAL YOGA DAY” celebration
Mode of Conduct: Online



Date: 24/06/2021 Event Name: Webinar on “Prepare You Before Start”

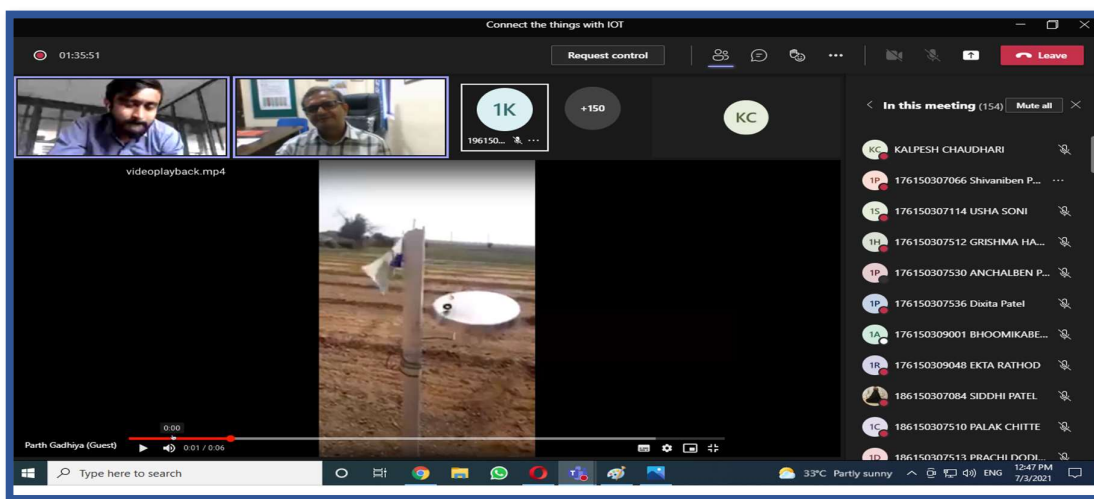
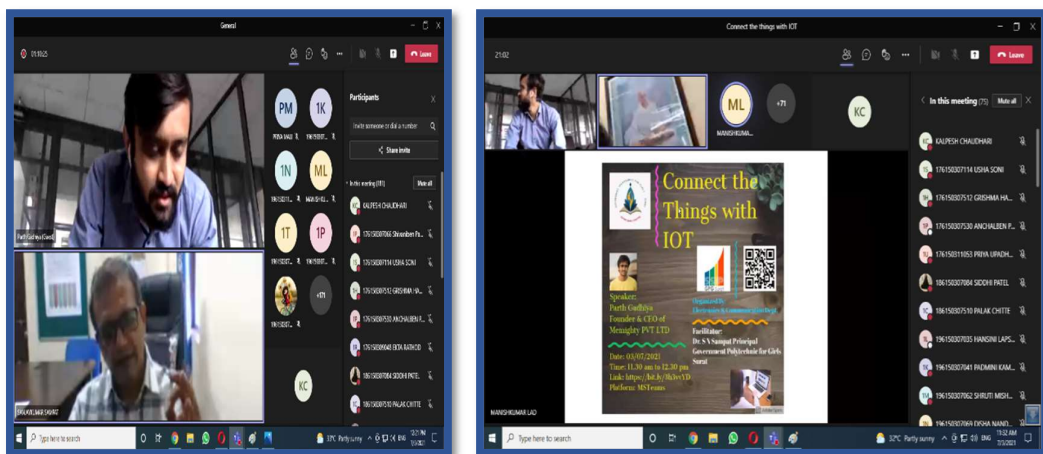
**DATE: 02/08/2021 EVENT NAME : EXPERT LECTURE BY MINAXI TRIPATHI
ON “ FOOD & NUTRITION “ Mode of Conduct: Online**



DATE: 15-08-2021 EVENT NAME: Independence Day Celebration



Date: 03-07-2021 expert lecture by Mr. Parth Ghadiya, Founder and CEO of Memighty PVT.LTD on “ **Connect the Things with IOT**” online on MS TEAM.



Date: 21-08-2021 Event Name: Tree plantation activity



Date: 26/08/2021 COVID VACCINATION @ GGP. Surat S.P. hall



**Date: 04/09/2021 Event Name: Webinar on "Basics of Raspberry PI" By EC STAFF
FOR 6th Sem EC DEPARTMENT, Mode of Conduct: ONLINE**

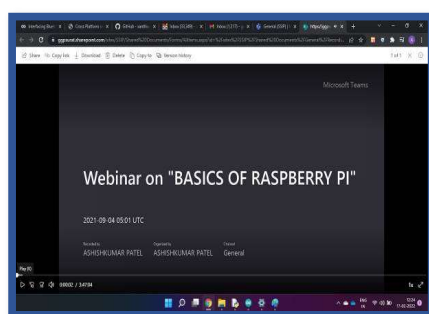
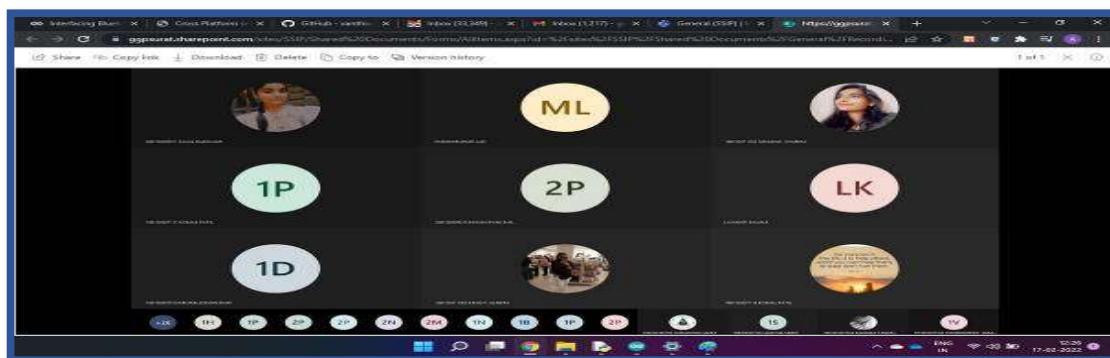
VISION
To become a premier diploma engineering institute that empowers girls to make it in industry and serve the society.

Mission
1. To strive for academic excellence and professional competence among students and staff.
2. To create a conducive campus environment for exchange of ideas and knowledge.
3. To initiate and adopt policies for skill development and innovation, with emphasis on entrepreneurship.
4. To provide the best responses and infrastructure.

ORGANIZED BY
EC Department,
Government Polytechnic
For Girls, Surat
Link for joining(MS Teams):
<https://bit.ly/3eGBDrC>
Speaker: A. M. Patel (Lecturer in EC)
Coordinator: K. P. Chaudhari (Lecturer in EC)

WEBINAR ON "BASICS OF RASPBERRY PI"
4th September 2021
10:30 AM to 11:30 AM

Hosted by:
Dr. P. S. Sasipriya
Principal
Government Polytechnic For Girls, Surat



Webinar on Jan Andolan for “covid -19 Awareness “ by Dr. prakash kyada

GOVERNMENT POLYTECHNIC FOR GIRLS, SURAT
Organized by National Service Scheme (NSS)
Webinar on Jan Andolan for 'Covid-19' Awareness

coordinator: Shobhana Malviya
Lecturer in Maths,
NSS Coordinator, GPG, Surat

Facilitator: Dr.S.N. Sampat
Principal of
GPG College,
Surat

Speaker: Dr. Prakash Kyada
Cardiologist,
Consulting Physician,
NCD Medicine
(Mumbai)

DATE TIME **24-October-2020**
1:00 to 2:00 pm

Webinar on Google meet
to join please register
through the QR code

Not Me But You..
Prepared by NSS volunteer: Rajput Manisha M



Student Result in GTU With Highest

SR. NO.	SEMESTER	ENROLLMENT NO	STUDENTS NAME	SPI
1	2	206150311002	PADHIYAR KOMALBEN SURESHBHAI	9.39
2	2	206150311005	RIYA PATEL	9.39
3	2	206150311003	RAJAK KAJAL RAJU	9.39
4	4	196150311005	GANDHI KESHVI HIMANSHUBHAI	9.5
5	4	196150311038	YADAV SONI RAJENDRA	9.2
6	4	196150311004	CHAUDHARI SEJALKUMARI RATILALBHAI	9.17
7	6	166150311090	RANA HIRAL VINODKUMAR	9.8
8	6	156150311049	KUSHWAHA NIDHI SUMAN	9.4
9	6	176150311054	VAGHANI PANKTI NATUBHAI	9.33